Development of Soft Error Simulator Based on Layout Information

Takuya Teraoka, Yuji Nakamura, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga and Toshinori Sueyoshi
Graduate School of Science and Technology, Kumamoto University
2-39-1 Kurokami, Chuo-ku, Kumamoto 860-8555, Japan
Email: {amagasaki, iida, kuga, sueyoshi}@cs.kumamoto-u.ac.jp, {teraoka, nakamura}@arch.cs.kumamoto-u.ac.jp

I. Introduction

With scaling down of semiconductor devices and the development of high integration density, large scale integration (LSI) designs are becoming more complex and longer design cycles are required. Field-programmable gate arrays (FPGAs) are used widely as a solution to the above problems, due to their programmability after manufacturing. However, the large quantity of configuration memory bits used for logic, routing make FPGA more undependable when single event upset (SEU) occurs. Particularly, static RAM (SRAM) based FPGAs are more vulnerable to soft errors since a radiation strike in configuration memory bits have a permanent effect on the system. Since configuration memory bits constitute the majority of SRAM cells in FPGA devices (e.g. more than 80% for Xilinx Virtex-6 VLX240T device [1]), the protection of configuration memory bits against multi bit upsets (MBUs) is of very important. Several countermeasures have been proposed to address the SEU. Triple modular redundancy (TMR) can shadow soft error concurrently but has over three times area overhead, which is critical to reconfigurable devices.

We propose soft error simulator developed to calculate bit interleaving distance. Our simulator calculates soft error patterns and occurrence probability which include multi bit errors in the SRAM array. Based on the obtained bit interleaving distance, we actually design FPGA layout and perform evaluation. The rest of the paper is organized as follows: The existing approaches to mitigate SEU are presented in Section 2. The proposed soft error simulator that is used to reveal MBU pattern is shown in Section 3. The evaluation details and the experimental results are provided in Section 4. Finally, the paper is concluded in Section 5.

II. Preceding Work

TMR is the most historical error mitigation method. We can find the use of the TMR in almost all the high reliability required field. Thus, the performance of TMR has become a base line for new proposed error mitigation techniques. TMR can mitigate one error upset in each redundant circuit but cannot correspond to MBU and has over 300% area overhead.

Bit interleaving techniques eliminate MBU events in SRAMs from a single particle hit [2]. Figure 1 show how bit interleaving has advantageous when an MBU occurs using TMR as an example. In a bit-interleaved memory (Fig. 1), physically adjacent memory cells are mapped to different error correct circuits. If the bit interleaving distance is greater than the spread of a MBU, it results in multiple SBUs in multiple error correct circuits instead of an MBU.

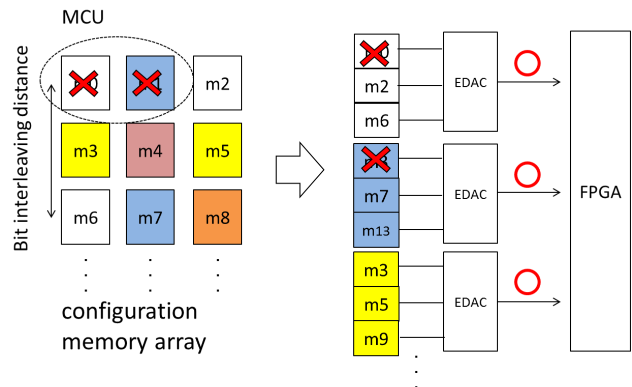

Fig. 1. Example of MBU concealment using bit interleaving technique

III. Soft Error Simulator

A. MBU site extraction using monte-carlo simulation

To calculate bit interleaving distance, MBU pattern on SRAM is needed. In this work, we developed the soft error simulator for the MBU pattern according to [3]. In this technique, the surface affected by a particle in configuration memory arrays is estimated with oval shapes obtained from available MBU patterns derived by actually collided radiation. Considering MBU patterns occurrence probability, ovals are randomly placed at different locations inside the memory array and the list of affected cells are extracted. Predominant MBU patterns in memory arrays have been comprehensively studied using neutron beam based accelerated SER estimation[4]. Most of the MBU patterns can be effectively covered by an oval surface as shown in Fig. 2. Only a subset of cells which have an overlap with the oval surface are considered as error sites.

B. Soft Error Detection

The way of detecting soft errors is in a similar manner as [3]. Figure 3 represents how sensitive zones for a SRAM layout are extracted. A cell has overlap with an oval surface if at least one of the sensitive zones to soft errors (N-diffusion and P-diffusion) falls within the surface. When a particle strikes a cell, it causes the additional charge to be collected in the diffusion parts of the transistor which in turn disturbs the normal operation of the transistor. The charge collected to the diffusion parts which are connected to VDD and GND pins is evacuated and does not affect the circuit behavior. The other parts of the diffusion can be disturbed by collection of

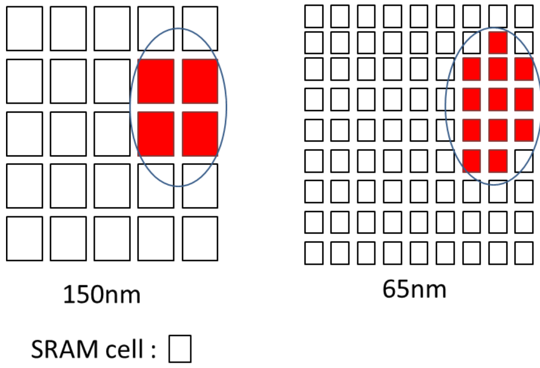

Fig. 2. Extraction of MBU sites from existing actual measurement MBU patterns

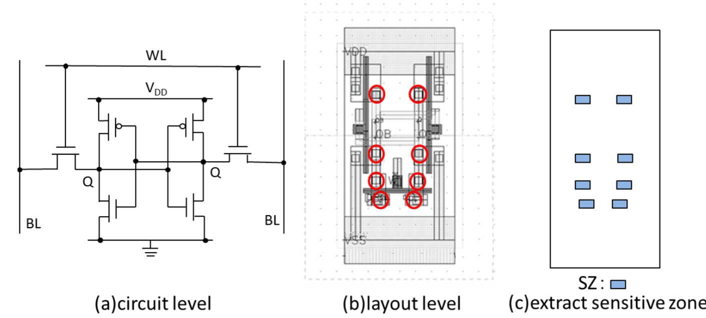

Fig. 3. Sensitive Zone (SZ) extraction for a NAND gate cell layout

additional charge. The oval shapes also are characterized based on actual measurement.

C. Simulation flow

Figure 4 shows overall flow of our simulator. Initially, the list of ovals and their occurrence probability are extracted from existing MBU patterns and then a sensitive zone is characterized for identification of soft error. Then, it is checked whether it has an overlap with the oval surface and the list of cells overlapped by the oval surface is extracted as shown in the right of Fig. 4. At the end, soft error pattern and probability are extracted.

IV. EVALUATION

In this section, we explore the bit-interleaving distance using soft error simulator. We used an SRAM device processed with 65nm technology. Figure 5 shows MBU patterns and probability of occurrence. In this evaluation, we generate injection ellipses with 22, 47, 95 and 144 Mev energy[4]. As it can be seen, the maximum MBU dimension is 4×2. In the case of 22MeV, about 80% of the SRAM soft errors are SBU incidents. We must not neglect the MBU measures in such case in order to increase the soft error tolerance. As a results, the interleave distance which can conceal all MBU patterns is 4. Based on this distance, we actually perform the FPGA tile layout using standard cell library.

V. CONCLUSION

In this paper, we proposed soft error simulator developed to calculate bit interleaving distance. As a result, the interleave distance which can conceal all MBU patterns was 4. Therefore, we can search a bit interleaving distance by using this simulator. In the future, we will to further improve accuracy.

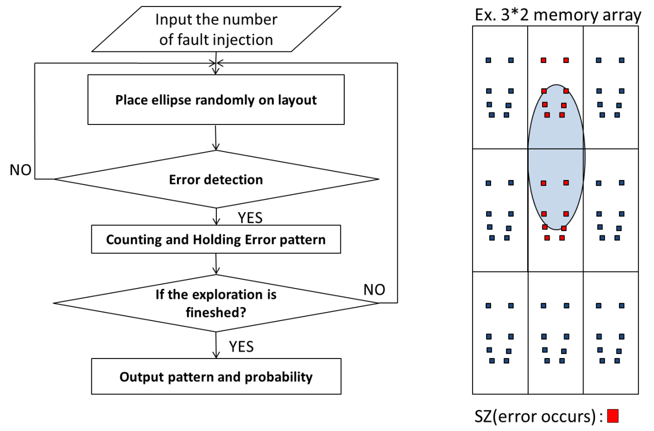

Fig. 4. Simulation flow chart

pattern							
number	1	2	3	4	5	6	7

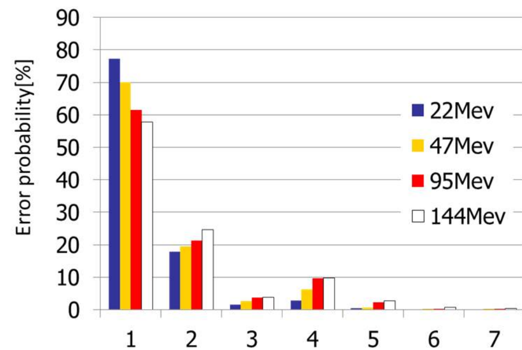

Fig. 5. MBU patterns and probability

References

[1] Parthasarathy M.B. Rao, Mojtaba Ebrahimi, Razi Seyyedi and Mehdi B. Tahoori, "Protecting SRAM-based FPGAs Against Multiple Bit Upsets Using Erasure Codes," Proc of DAC2014, pp.1-6, June. 2014.

[2] Nilesh Badodekar, "Mitigating Single-Event Upsets Using Cypress ' s 65-nm Asynchronous SRAM," Cypress white paper, Document No. 001-88889

[3] Mojtaba Ebrahimi, Hossein Asadi and Mehdi B. Tahoori, "A Layout-based Approach for Multiple Event Transient Analysis," Proc of DAC2013, pp.1-6, May. 2013.

[4] Daniele Radaelli, Helmut Puchner, Skip Wong, and Sabbas Daniel, "Investigation of Multi-Bit Upsets in a 150 nm Technology SRAM Device," Proc of NPSS2005, pp.2433-2437, Dec. 2005.